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The Waveform Bounding Approach to Timing Analysis of Digital MOS IC's*

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# THE WAVEFORM BOUNDING APPROACH TO TIMING ANALYSIS OF DIGITAL MOS IC'S.

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## ABSTRACT

The waveform bounding approach to fast timing analysis of MOS VLSI circuits is discussed. The idea is to compute rigorous closed-form expressions giving upper and lower bounds for transient voltage waveforms, rather than exact values. The goal is to enable rapid computation without sacrificing user confidence in the results.

## I. Background and Objectives

Existing approaches to timing analysis and simulation of digital integrated circuits fall, roughly speaking, into three classes:

i) Methods such as SPICE2 [1] and ASTAP [2], based on essentially exact numerical solution of the network's differential equations, are accurate and reliable. But even with the increase in speed afforded by the waveform relaxation method [3], exact numerical solution is too slow for the needs of the VLSI era.

ii) *Specialized MOS timing simulators* like MOTIS-C [4] and SPLICE [5] rely on table look-up of device characteristics for speed, and save additional time by terminating a Newton-Raphson or similar iteration before convergence is reached. SPLICE is in addition a mixed-mode circuit, timing and logic simulator and uses a selective trace algorithm to exploit latency. In both these programs the termination of an iterative step prior to convergence saves time at the cost of accuracy and, in some instances, of numerical stability [6]. The improvement in speed over SPICE2 is typically one to two orders of magnitude for SPLICE [5] and about two orders of magnitude for MOTIS-C [7].

iii) More recently, some researchers are exploring an alternate approach to timing analysis and simulation based on a radically simplified electrical description of the network. RSIM [8], CRYSTAL [9], and TV [10,11] fall at the far end of the speed-accuracy tradeoff curve from SPICE2. A MOSFET is typically represented in these programs by an extremely simplified model: a linear resistor in series with a switch. And a polysilicon or diffusion line is represented by a lumped capacitance in RSIM, or by a delay in TV obtained by simply averaging the upper and lower delay bounds obtained by Rubinstein, Penfield, and Horowitz [12]. These programs are potentially very fast and have a number of attractive user-oriented features. The drawback, of course, is that there are no absolute known limits to the error in their total delay estimates. The user can never be sure the answers they give are close enough.

The objective of the waveform bounding approach to timing analysis and simulation is to combine the computational speed that results from avoiding the numerical solution of differential equations with the user confidence in the result that comes from rigorous uncertainty bounds. Our attack on the timing analysis problem is based on a careful fundamental study of the differential equations describing the dynamics of gates, pass transistors, interconnect, and the standard digital circuits constructed from them.

In addition to the MIT group working on this project, Mark Horowitz [12,13] is currently completing a dissertation on MOS timing analysis at Stanford.

## II. Response Bounds for Interconnect

### 2.1) Linear Interconnect Models

This section summarizes the results obtained in [12]. In this work an MOS signal distribution network as shown in Fig. 1 is modelled as a branched linear RC line, i.e., an RC tree, as in Fig. 2.

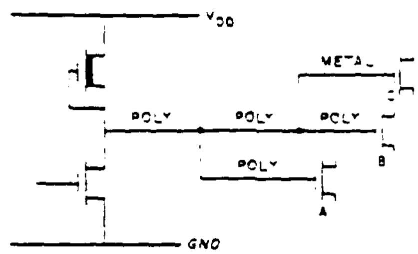


Figure 1. Typical MOS signal-distribution network. The inverter is shown driving three gates.

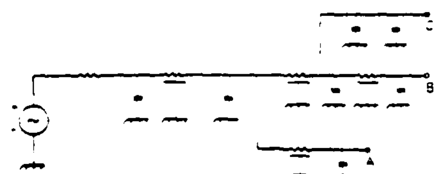


Figure 2. The linear RC tree shown above is a model for the network of Fig. 1. The voltage source is a unit step at time $t = 0$.

For any two nodes in the network, $R_{\ell m}$ is defined as the sum of the resistances along the route consisting of the intersection of the path from the input to node i with the path from the input to node m, as illustrated in Fig. 3. The three time

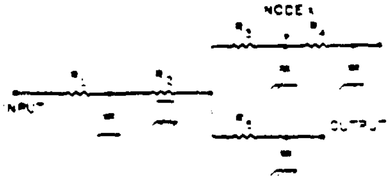

Figure 3. Illustration of resistance terms. For this network, $R_{ki} = R_1 + R_2$, $R_{kk} = R_1 + R_2 + R_3$, and $R_{ii} = R_1 + R_2 + R_5$.

constants used to derive response bounds are

$$T_P \triangleq \sum_k R_{kk} C_k \tag{1}$$

$$T_{Di} \triangleq \sum_k R_{ki} C_k \tag{2}$$

$$T_{Ri} \triangleq \sum_k (R_{ki}^2 C_k)/R_{ii} \tag{3}$$

where the summations are taken over all nodes of the network. The derivation in [12] shows that $\underline{v}_i(t) \le v_i(t) \le \bar{v}_i(t)$, for all $t \ge 0$, where $v_i(t)$ is the actual zero state step response at any terminal node i, and the bounds $\underline{v}_i(t)$ and $\bar{v}_i(t)$ are given by

$$\underline{v}_i(t) \triangleq \begin{cases} 0, & 0 \le t < T_{Di} - T_{Ri} \\ 1 - \frac{T_{Di}}{t + T_{Ri}}, & T_{Di} - T_{Ri} \le t < T_P - T_{Ri} \\ 1 - \frac{T_{Di}}{T_P} \exp[(T_P - T_{Ri} - t)/T_P], & T_P - T_{Ri} \le t \end{cases} \tag{4}$$

$$\bar{v}_i(t) \triangleq \begin{cases} 1 - \frac{T_{Di} - t}{T_P}, & 0 \le t < T_{Di} - T_{Ri} \\ 1 - \frac{T_{Di}}{T_P} \exp[(T_{Di} - T_{Ri} - t)/T_{Ri}], & T_{Di} - T_{Ri} \le t. \end{cases} \tag{5}$$

as illustrated in Fig. 4.

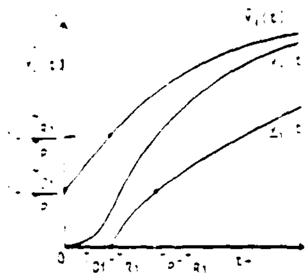

Figure 4. Form of the bounds with the distance from the exact solution exaggerated for clarity.

The time required to compute these bounds grows only linearly with the number of elements in the network. Recent applications of this result include [10,11,14,15 16]. The ultimate goal of this portion of the project is to derive a hierarchy of such bounds, permitting the user to trade off accuracy for computation time.

## 2.2) Nonlinearities Affecting Interconnect

The linear circuit model in Fig. 2 fails to incorporate three types of nonlinearities present in Fig. 1 or related circuits: the nonlinear output resistance of the inverter, the nonlinear gate-to-channel capacitance of the MOSFET loads, and the nonlinear capacitance from any diffusion line to substrate. This section describes recent work [17-20] that allows the bounds for linear networks [12] to be applied to RC lines incorporating such nonlinearities. (Further research is needed for branched lines, i.e. RC trees.)

Using the notation and sign conventions illustrated in Fig. 5, the

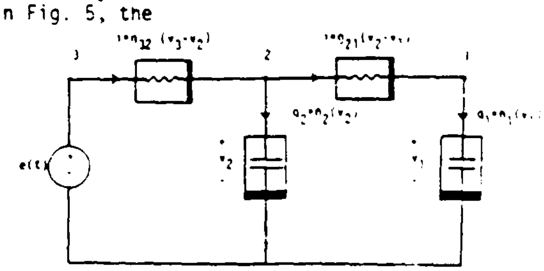

Figure 5. Two-capacitor example of a nonlinear, nonuniform RC line.

state equations for any nonuniform, nonlinear lumped RC line with N capacitors can be written in the form

$$\dot{v}_j = \frac{1}{C_j(v_j)} \left[ g_{j+1,j}(v_{j+1} - v_j) - g_{j,j-1}(v_j - v_{j-1}) \right], \quad 1 \le j \le N, \tag{6}$$

where $g_{10} \triangleq 0$, $v_{N+1} \triangleq e$, and the capacitor constitutive relations $q_j = h_j(v_j)$ are continuously differentiable with $C_j(v_j) \triangleq h_j'(v_j) > 0$ everywhere. We assume the resistor curves are continuously differentiable, strictly increasing, and pass through the origin.

<u>Lemma 1 [19]</u>

Consider any nonlinear, nonuniform RC line. At any instant during an "up" transition (i.e. $e \ge 0$, $\dot{e} \ge 0$) from equilibrium,

$v_j(t) \ge 0$, $v_j(t) \le e$, $v_j(t) \le v_{j+1}(t)$
and $\dot{v}_j(t) \ge 0$, $1 \le j \le N$.

Lemma 1 is proved in [19]. Using it, we give a proof in [20] of the

<u>Monotone Response Theorem for Nonlinear, Nonuniform RC Lines.</u> Given a nonlinear RC line as described above. Suppose that (because of circuit parameter uncertainty, the use of linearized models for nonlinear elements, replacing the exact input by input bounds, etc.,) we do one or more of the following:

a) overestimate the input e(t),

b) underestimate one or more R's,

c) underestimate one or more C's.

The resulting circuit model will then necessarily <u>overestimate</u> the output $v_j(t)$ at each instant t during "up" transitions (i.e., during transitions where $e \ge 0$, $\dot{e} \ge 0$ throughout.)

A similar result holds for "down" transitions and estimate errors of the opposite sign. Using part a) of the assumptions, this theorem allows us to computationally propagate upper and lower signal bounds through the network. Using parts b) and c), it allows us to replace a nonlinear line by two linear ones, one strictly faster and one strictly slower, to which the linear network bounds (4,5) in turn apply. We have not yet succeeded in finding a generalization of this result that will apply to non-linear RC trees.

## III. An Approach to Waveform Bounding for MOS Logic Gates

The results reported here apply to MOS device models of the form

$$i_D = \frac{W}{L} f(v_{GB}, v_{DB}, v_{SB}), \qquad (7)$$

where D,G,S and B refer to drain, gate, source and substrate, respectively. For specificity we consider only n-channel devices in this paper. No special algebraic form for f is assumed, only that f is continuously differentiable and satisfies the natural monotonicity conditions

$$\frac{\partial f}{\partial v_{GB}} \geq 0, \ \frac{\partial f}{\partial v_{DB}} \geq 0, \ \frac{\partial f}{\partial v_{SB}} \leq 0 \qquad (8)$$

everywhere. Thus a wide variety of device models are allowed, with the exception that (7) does not allow for short-channel effects.

Our approach will be to reduce a multiple-input logic gate by steps to an "equivalent bounding inverter" and then to find bounds for the response of this inverter.

### 3.1) Reduction of Series-Parallel Transistor Network to "Equivalent Bounding Transistor"

We have developed a method for reducing any series-parallel transistor network to a single "equivalent bounding transistor." Using the technique recursively, one can replace the pullup or pulldown network of a multiple-input gate by a single transistor and have rigorous bounds for the error produced by this simplification.

For example, a parallel connection of N transistors, all identical except for widths, lengths and gate voltages, satisfies

$$i = f(\vec{v}_{GB}, v_{DB}, v_{SB}) \triangleq \sum_{j=1}^{N} \frac{W_j}{L_j} f(v_{GB_j}, v_{DB}, v_{SB}), \qquad (9)$$

where $\vec{v}_{GB}$ is the vector of gate voltages. We have proven that, because of the assumptions (8), there exist $W_{eq}$, $L_{eq}$ independent of $\vec{v}_{GB}$, and $\underline{v}_{GB}$ and $\overline{v}_{GB}$ that depend on $\vec{v}_{GB}$ such that (9) can be replaced by the simpler bounds

$$\frac{W_{eq}}{L_{eq}} f(\underline{v}_{GB}, v_{DB}, v_{SB}) \leq i \leq \frac{W_{eq}}{L_{eq}} f(\overline{v}_{GB}, v_{DB}, v_{SB}), \qquad (10)$$

for all $v_{DB} \geq v_{SB}$, describing a single transistor with a range of gate voltages. The function f is the same throughout (9) and (10). Figure 6 illustrates this process for N = 2.

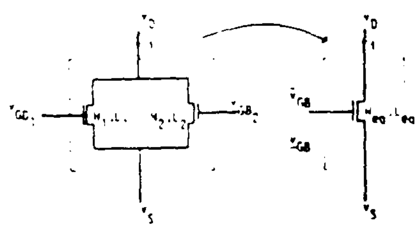

Figure 6. Replacing a parallel transistor network by an "equivalent bounding transistor". The cost of this simplification is that the exact value of i for the network on the left is replaced by a range of values in the simpler model corresponding to $\underline{v}_{GB} \leq v_{GB} \leq \overline{v}_{GB}$.

### 3.2) Reducing a Multiple-input Gate to an "Equivalent Bounding Inverter"

A gate can be modelled as an "equivalent bounding inverter" by performing the reduction outlined in section 3.1 on both the pullup and pulldown networks, reducing each to a single transistor. Initial trials, comparing SPICE2 simulations of the original network with simulations of the "equivalent bounding inverter" indicate that the resulting bounds for $i_{out}(v_{out})$ differ from the exact values by only about $\pm$ 10% for practical circuits.

### 3.3) Bounding the Response of an Inverter and Load to Input Transitions

When applied to some multiple-input gates, the reduction procedure described in the previous two subsections may yield an inverter in which the pullup gate is externally driven. But for simplicity we consider here only the case of a standard NMOS depletion - load inverter as in Fig. 7.

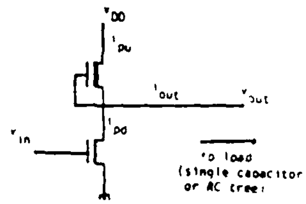


Figure 7. Depletion-load inverter.

To bound the response time of the loaded inverter we need simple bounds on the function $i_{out}(v_{out}, v_{in})$, which is the difference of the pullup and pulldown currents:

$$i_{out}(v_{out}, v_{in}) = i_{pu}(v_{out}) - i_{pd}(v_{out}, v_{in}). \qquad (11)$$

Simple linear bounds on both the pullup and pulldown currents are shown in Fig. 8. The resulting bounds for the output curve $i_{out}(v_{out})$ depend on $v_{in}(t)$.

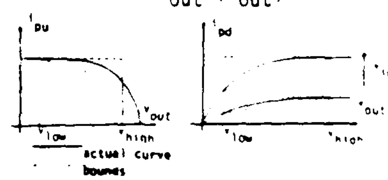


Figure 8. Simple linear bounds on the pullup and pull-down currents. The latter depend on $v_{in}$, and hence on t.

Initial simulations using this approach indicate that the delay bounds for these simplified models differ from the delays obtained from SPICE simulations by about $\pm$ 15%.

## IV. Further Work in Progress

Much work remains to be done before the theoretical basis for the waveform bounding approach to timing analysis is complete. Among the larger remaining problems are:

1. extending the Penfield-Rubinstein bounds to incorporate time-varying source resistances, such as those modelling the pulldown current in Fig. 8,

2. finding bounds for the response of an RC tree containing pass transistors,

3. investigating the tolerance in the bounds obtained so far and finding tighter ones where necessary, and

4. incorporating effects of the Miller capacitance into bounds.

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